



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/024,088	12/17/2001	Matthew A. Hayduk	ITL.0649US (P12390)	3752
7590	12/12/2005		EXAMINER	
Timothy N. Trop TROP, PRUNER & HU, P.C. STE. 100 8554 KATY FWY. HOUSTON, TX 77024-1805			SONI, DEEPAK H	
			ART UNIT	PAPER NUMBER
			2668	
DATE MAILED: 12/12/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/024,088	HAYDUK ET AL.
	Examiner	Art Unit
	Deepak Soni	2668

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 12/17/2001.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-28 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-28 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ . |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ . | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ . |

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
2. Claims 1 - 4 and 18 - 21, are rejected under 35 U.S.C. 102 (e) as being anticipated by Masunaga et al. (Pub No: US 2002/0105977). The Masunaga et al. reference teaches all of the limitations of the listed claims with reasoning that follows.

Regarding Claims 1 and 18, "establishing a serial physical link and providing isochronous support" (In the IEEE 1394 high performance serial bus standards, the transfer operation that occurs within a network is called a sub-action. For this sub-action, there are defined two transfer modes: an asynchronous transfer mode called asynchronous and a synchronous transfer mode called isochronous in which the transfer band is assured as spoken of on page 1, paragraph 0013) "which by a software control on the serial physical link" (The firmware comprises a transaction layer consisting of a management driver for performing actual operations for the interface conforming to the IEEE 1394 standards, and a management layer consisting

of a management driver conforming to the IEEE 1394 standards called a serial bus management (SBM) as spoken of on page 1, paragraph 0011).

Claim 18 having a further limitation of "logical layer control to interface with said physical link" (Figure 3 shows physical layer interface with link layer).

Regarding **Claims 2 and 20**, "providing synchronous support by a software control on the serial physical link" (In the IEEE 1394 high performance serial bus standards, the transfer operation that occurs within a network is called a sub-action. For this sub-action, there are defined two transfer modes: an asynchronous transfer mode called asynchronous and a synchronous transfer mode called isochronous in which the transfer band is assured as spoken of on page 1, paragraph 0013) "which by a software control on the serial physical link" (The firmware comprises a transaction layer consisting of a management driver for performing actual operations for the interface conforming to the IEEE 1394 standards, and a management layer consisting of a management driver conforming to the IEEE 1394 standards called a serial bus management (SBM) as spoken of on page 1, paragraph 0011).

Regarding **Claims 3 and 19**, "providing asynchronous support by a software control on the serial physical link" (In the IEEE 1394 high performance serial bus standards, the transfer operation that occurs within a network is called a sub-action. For this sub-action, there are defined two transfer modes: an asynchronous transfer mode called asynchronous and a synchronous transfer mode called isochronous in which the transfer band is

assured as spoken of on page 1, paragraph 0013) “which by a software control on the serial physical link” (The firmware comprises a transaction layer consisting of a management driver for performing actual operations for the interface conforming to the IEEE 1394 standards, and a management layer consisting of a management driver conforming to the IEEE 1394 standards called a serial bus management (SBM) as spoken of on page 1, paragraph 0011).

Regarding Claim 4, “providing separate logical and physical layers” Figure 3 shows a separate physical layer and link layer.

Regarding Claim 21, “physical layer control is coupled to said logical layer control” (Figure 3 shows physical layer interface with link layer).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5 - 7 and 23 - 24, are rejected under 35 U.S.C. 103(a) as being unpatentable over Masunaga et al. (Pub No: US 2002/0105977) in view of Sarkar (VLSI 2000: Digital Imaging with Wireless Data Services)

Regarding Claims 5 and 22, Masunaga does not teach “providing a multiplexer in the physical layer coupled to the logical layer” Sarkar teaches

cdma2000 layering where multiplexing of the logical channels form/to different physical channels based on the Logical to physical mapping table as shown in Figure 11 and spoken of on page 6, paragraph 1. At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references to combine isochronous, synchronous and asynchronous streams and multiplexing them at physical layer. A motivation for doing so would be for supporting higher speed data, useful for imaging as spoken on page 6 in Conclusion paragraph of Sarkar reference.

Regarding Claims **6 and 23**, Masunaga does not teach “coupling a baseband processor to said physical layer” Sarkar teaches a Conceptual diagram of MSM3000 where CDMA processor is integrated in a phone as shown in Figure 9 and as spoken of on paragraph 2 on page 5. At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references to handle CDMA protocol via CDMA processor to allow the application processor to support more data intense tasks. A motivation for doing so would be for supporting higher speed data, useful for imaging as spoken on page 6 in Conclusion paragraph of Sarkar reference.

Regarding Claims **7 and 24**, Masunaga does not teach “coupling an applications processor to said physical layer” Sarkar teaches a Conceptual diagram of MSM3000 where Micro processor subsystem is integrated in a phone as shown in Figure 9 and as spoken of on paragraph 2 on page 5. At the time of the invention, it would have been obvious to someone of ordinary

skill in the art given these references to handle Data intense task via application processor to allow CDMA processor to handle CDMA protocol tasks. A motivation for doing so would be for supporting higher speed data, useful for imaging as spoken on page 6 in Conclusion paragraph of Sarkar reference.

5. Claims **8 - 17 and 25 - 28**, are rejected under 35 U.S.C. 103(a) as being unpatentable over Masunaga et al. (Pub No: US 2002/0105977) in view of Sebire et al. (Pub No: US 2004/0120302) and in further view of Wu et al. (R.O.C. ministry of Economic Affairs under the project No. 3P12200 conducted by ITRI: Integrated Traffic Control for Multimedia Communications over Packet Switched Networks).

Regarding Claims **8 and 25**, Masunaga does not teach “providing a plurality of different channel mapping schemes and enabling the selection of one of said schemes” Wu teaches Multiplexing is an essential function in all kinds of communication networks. There are two levels of multiplexing in packet networks, physical layer multiplexing and packet layer multiplexing. At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references to combine multimedia streams and multiplexing them at physical layer and at logical layer. A motivation for doing so would be efficient traffic control for multiplexing a plurality of packets

streams with different grade of services as spoken of in Abstract of Wu reference.

Regarding Claims **9 and 26**, Masunaga does not teach “providing a channel mapping scheme in which each of a plurality of classes has its own channel” Sebire teaches classes having dedicated channels as spoken of on page 4, paragraph 0060 and page 13, paragraph 0177 and 178) “and multiplexing logical channels with the same priority in round robin fashion” Sebire and Masunaga fail to teach multiplexing logical channels and priority in round robin. However Wu teaches packet layer multiplexing which deals with multiplexing of various logical channels over the line as spoken of on page 1 paragraph 2. Wu also teaches traffic scheduling method Dynamic Weighted Round-Robin for two types of traffic streams, namely sensitive streams and the best-effort streams. At the time of the invention, it would have been obvious to someone of ordinary skill in the art given these references to combine and implements the traffic class channel that deals with conversational, background and stream data and multiplex logical channels in priority scheme. A motivation for doing so for providing efficient traffic control for multiplexing a plurality of packets streams with different grade of services as spoken of in Abstract of Wu reference.

Regarding Claims **10 and 27**, Masunaga does not teach “dynamically assigning channels on a first come, first served basis” Wu teaches states 1,2, and 3 and its priority in round robin priority as spoken of in Section 3:The

Scheduling Algorithm on page 3 and 4. At the time of the invention, it would have been obvious to someone of ordinary skill in the art to use some type of priority schedule to service the data stream. A motivation for doing so for providing efficient traffic control for multiplexing a plurality of packets streams with different grade of services as spoken of in Abstract of Wu reference.

Regarding Claims **11 and 28**, Masunaga and Wu do not teach “assigning a plurality of channels to conversational service and providing a plurality of multiplexed channels for other services” Sebire teaches multiplexing scenarios for conversational traffic class and background traffic class as spoken of on page 2 paragraph 0021-0029. At the time of the invention, it would have been obvious to someone of ordinary skill in the art to use the operational scenarios for conversational and background traffic as in Sebrie. A motivation for doing so for providing efficient traffic control for multiplexing a plurality of packets streams with different grade of services as spoken of in Abstract of Wu reference.

Claims **12 and 13**, do not substantially differ from claim 1 and 2 except it recites “medium storing instructions that enable a processor-based system” Masunaga and Wu do not teach storing instruction that enable processor-based system. However Sarkar teaches system having a Microprocessor Subsystem and Peripheral Circuits (RAM, ROM, EEPROM ect.) as shown in Figure 9, page 5. At the time the invention was made it would have been obvious to translate steps into instruction for use by the microprocessor of

Sarkar. One of ordinary skill in the art would be motivated to do this for the efficiency due to automated system. (See Claims 1 and 2 for further explanation)

Claims 14 - 17, do not substantially differ from claim 8-11 except it recites "medium storing instructions that enable a processor-based system" Masunaga and Wu do not teach storing instruction that enable processor-based system. However Sarkar teaches system having a Microprocessor Subsystem and Peripheral Circuits (RAM, ROM, EEPROM ect.) as shown in Figure 9, page 5. At the time the invention was made it would have been obvious to translate steps into instruction for use by the microprocessor of Sarkar. One of ordinary skill in the art would be motivated to do this for the efficiency due to automated system. (See Claims 8 – 11 for further explanation)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Deepak Soni whose telephone number is 571-272-2816. The examiner can normally be reached on 9:00Am - 5:00Pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Deepak Soni
Examiner
AU: 2668

DS



FRANK DUONG
PRIMARY EXAMINER